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Our Docket No.: 080398.P115

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	08/936,344	Confirmation No. 9648
Applicant	:	Paul Michael Embree et al.	
Filed	:	September 24, 1997	
TC/A.U.	:	2644	
Examiner	:	Minsun Oh Harvey	
Docket No.	:	080398.P115	
Customer No.	:	8791	

APPEAL BRIEF

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

Dear Sir:

Applicants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicants also submit herewith our check number 14721 in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(f). Please charge any additional fees or credit any overpayment to our deposit Account No. 02-2666.

02/11/2004 BDAVENPO 00000002 022666 08936344
01 FC:1251 110.00 DA

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01 FC:1402 330.00 OP

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I. REAL PARTY IN INTEREST

The real parties in interest are the assignees, Sony Corporation and Sony Pictures Entertainment, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-15 of the present application are pending and remain rejected. The Applicants hereby appeal the rejection of claims 1-15.

IV. STATUS OF AMENDMENTS

The Applicants filed an amendment on May 28, 2003, in response to an Office Action issued by the Examiner on February 5, 2003. In response to the May 28, 2003, amendment, the Examiner issued a Final Office Action on August 12, 2003, maintaining the rejection. The Applicants filed a Notice of Appeal on October 13, 2003.

V. SUMMARY OF INVENTION

The present invention discloses a technique to allocate memory for real-time audio processing. A system 100 includes a plurality of embedded boxes (EBX's) for processing audio signal and audio engineering society (AES) standard input/output channels 125.

Each of the EBXes includes at least one or more processors 205, a signal processing subsystem 270, and a SCSI-2 controller 250_1.[1] The signal processing system includes a memory system 300.[2] The memory system 300 includes two 2-to-1 multiplexers MUX0 310 and MUX1 311 and two dynamic random access memory (DRAM) banks BANK0 320 and BANK1 321.[3] MUX0 310 and MUX1 311 are connected to the digital signal processor (DSP) bus and the Peripheral Component Interconnect (PCI) bus and to the DRAM BANK0 320 and BANK1, respectively. The SCSI-2 controller 2501 is connected to the PCI bus.[4] Each of the MUX0 310 and MUX1 311 consists of two multiplexers: address multiplexer and data multiplexer.[5] MUX0 310 and MUX1 311 are controlled by the SEL0 and SEL1 signals, respectively. When SEL0 and SEL1 are at a first logic level, the data transfer is between the selected DRAM bank and the PCI bus to the SCSI controller 250_1. When SEL0 and SEL 1 are at a second logic level, the data transfer is between the selected DRAM bank and the DSP bus.[6] DRAM BANK0 320 and DRAM BANK1 321 are two dynamic random access memory banks operating separately and independently.[7] By controlling the SEL0 and SEL 1, the two DRAM banks can be accessed simultaneously by two different processors. For example, the SCSI controller may access the DRAM BANK0 320 for storing data while the DSP is reading the data out from DRAM BANK1 321.[8] Audio signals are sampled at a sampling rate of 48 KHz. During each sampling period, 16 samples from 16 audio channels are received from the serial AES input ports and stored in the DRAM banks in recording mode. During the same sample period, the playback of the digital audio is done by reading the data stored in the DRAM banks and sending it to the serial AES output ports.[9]

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[1] See specification, page 5, lines 17-24; page 7, lines 1-25; page 7, lines 20-25; page 8, lines 1-6.
[2] See specification, page 8, lines 19-20.
[3] See specification, page 8, lines 21-23; page 9, lines 1-2.
[4] See specification, page 9, lines 1-3; Figure 3.
[5] See specification, page 9, lines 5-7; Figure 3.
[6] See specification, page 9, lines 12-16.
[7] See specification, page 9, lines 17-21.
[8] See specification, page 9, lines 22-25.
[9] See specification, page 10, lines 4-10; Figure 4.

The audio samples are allocated in the memory banks such that the storage of all audio channels is distributed equally over the entire memory banks. In general, each memory bank stores a subset of audio data which corresponds to a different group of audio channels. [10]

VI. ISSUE

The issue is whether Claims 2-4 and 6-15 are unpatentable under 35 U.S.C. §103 over U.S. Patent No. 4,636,942 issued to Chen et al. ("Chen") in view of International Application No. PCT/US89/05440 issued to Van Nostrand et al. ("Van Nostrand").

VII. GROUPING OF CLAIMS

Applicants contend that the claims of the present invention stand or fall together. In other words, claims 2-4 and 6-15 form a single group.

[10] See specification, page 11, lines 12-13.

VIII. ARGUMENTS

A. CLAIMS 2-4 AND 6-15 ARE UNOBVIOUS OVER CHEN IN VIEW OF VAN NOSTRAND

Claims 2-4 and 6-15 were rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,636,942 issued to Chen et al. ("Chen") in view of International Application No. PCT/US89/05440 by Van Nostrand et al. ("Van Nostrand"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness.

Chen discloses a computer vector multiprocessing control. A central memory is provided for two processors. Each processor has a respective data path and respective control path to the central memory (Chen, col. 4, lines 65-68). The two processors are identical and symmetric (Chen, col. 5, lines 50-51). The central memory is provided with eight ports, with four ports associated with each processor (Chen, col. 10, lines 31-32). There is no storage of real-time audio data associated with audio channels. Chen does not disclose, suggest, or render obvious memory banks storing subsets of audio data corresponding to different groups of audio channels.

Van Nostrand discloses a method and apparatus for handling high speed data. Video data are written into two banks of memory. Each bank is further divided into odd and even. Continuous data stream can be written into these two banks without interruption. Each of the memory arrays within each bank can be a video random access memory (VRAM). Memory arrays in bank A and bank B include shift registers (Van Nostrand, page 3). Van Nostrand merely discloses one stream of video data. A control circuit automatically selects odd/even pixel data to write to memory. The stream of video data of odd and even pixels are first routed to shift registers within one bank, bank A. Only

when bank A has been filled, the stream of video data is shifted to bank B (Van Nostrand, page 7).

Chen and Van Nostrand, taken alone or in any combination, does not disclose, suggest, or render obvious: (1) a plurality of memory banks having two memory banks accessible to first and second processors for operations selected from the group comprising read and write operations, and (2) storing subsets of audio data in the memory banks and the subsets corresponding to different groups of audio channels. The combination of Chen in view of Van Nostrand would teach away from the claimed invention in that it would teach or describe a computer vector multiprocessing with a control circuit provided to direct even data to one group of memory arrays within a bank and odd data to another group within that bank, and to switch the data stream between the banks.

There is no motivation to combine Chen and Van Nostrand because neither of them addresses the problem of memory allocation for real time audio processing. There is no teaching or suggestion that audio data from audio channels, plurality of memory banks, and storing subsets of audio data corresponding to different groups of audio channels are present. Chen, read as a whole, does not suggest the desirability of memory allocation by storing subsets of audio data corresponding to different groups of audio channels.

The Examiner stated that Van Nostrand disclosed using subsets corresponding to different groups of data channels, relying on the cited portion in Van Nostrand from page 4 (line 30) to page 5 (line 2) (Final Office Action, page 2-3). Applicants respectfully disagree. Van Nostrand merely discloses a technique to handle high speed data from a single source of image (Van Nostrand, page 4, lines 20-29). The cited portion merely states that bank A comprises memory arrays. The memory arrays have two groups. One group receives even data and another group receives odd data. Van Nostrand, therefore, differs from the claimed invention in at least three aspects. First, Van Nostrand does not

disclose different groups of channels, only digitized images. The data come from the same source, only to be divided into odd and even groups. Second, the memory banks are not accessible to first and second processors for operations selected from a group comprising read and write operations. Van Nostrand merely discloses a continuous stream of data in serial form (Van Nostrand, page 2, lines 16-19). The memory devices are designed only for receiving data, i.e., they are used for writing only. The reading is performed by using the shift registers (Van Nostrand, page 2, lines 18-24). Third, the data stream is for image data, not corresponding to audio data. The use of Video RAM (VRAM) is only suitable for pixel data, or image data.

Furthermore, combining Chen and Van Nostrand would render the prior art invention unsatisfactory for its intended purpose. If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01.

Here, Chen disclosed a central memory being segmented into thirty-two independently controllable banks (Chen, col. 11, lines 18-20). These banks are organized into four sections, each containing eight banks (Chen, col. 11, lines 20-21). Each of the four sections is provided with two independent access paths, each controlled by one of the CPU's, to the memory banks therewithin (Chen, col. 11, lines 25-28). On the other hand, Van Nostrand discloses two memory banks operating under control of a control means (Van Nostrand, page 2, lines 16-22). The control circuit alternately switches even data to the shift registers of even memory arrays and odd data to the shift registers of odd memory arrays (Van Nostrand, page 3, lines 24-29). Therefore, the two memory banks in Van Nostrand operate alternately, not as two independently controllable banks as disclosed in Chen.

Modifying Chen to incorporate the video memory arrays in Van Nostrand would render the multiprocessing unsatisfactory for its intended purpose. The intended purpose of the central memory organization in Chen is to provide independent and parallel accesses (Chen, col. 3, lines 44-50). Incorporating the video memory array organization in Van Nostrand would prohibit independent accesses from the two processors because the video memory arrays in Van Nostrand are alternately used to provide continuous stream without any interruption (Van Nostrand, page 3, lines 32-34; page 10, lines 25-31).

The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re ROUFFET, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a

convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

In the present invention, the cited references do not expressly or implicitly suggest (1) a plurality of memory banks having two memory banks accessible to first and second processors for operations selected from the group comprising read and write operations, and (2) storing subsets of audio data in the memory banks and the subsets corresponding to different groups of audio channels. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Chen and Van Nostrand is an obvious application of memory allocation for audio processing.

C. Conclusion

The Federal Circuit stated that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. In re Vaeck, 947 F.2d. 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Furthermore, M.P.E.P. § 2142 states that:

> "To establish a prima facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Here, Chen and Van Nostrand, taken alone or in any combination, does not disclose, suggest, or render obvious: (1) a plurality of memory banks having two memory banks accessible to first and second processors for operations selected from the group comprising read and write operations, and (2) storing subsets of audio data in the memory banks and the subsets corresponding to different groups of audio channels. Furthermore, the proposed modification would render the prior art invention, either from Chen or Van Nostrand, being modified unsatisfactory for its intended purpose.

As a result, none of the cited references discloses, suggests, or renders obvious the present invention as recited in claims 2-4 and 6-15.

Applicants respectfully request that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated or rendered obvious by the prior art.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: January 09, 2004

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (canceled)

2. (previously presented) The method of claim 3, further comprising selecting said memory banks for access by one of the first and second processors.

3. (previously presented) A method for allocating real-time audio data from a plurality of audio channels in a system having a first processor and a second processor, the method comprising:

providing a plurality of memory banks of semiconductor memory devices, each memory bank being accessible to the first and second processors for operations selected from the group comprising read and write operations, the plurality of memory banks includes two memory banks; and

storing subsets of said audio data in the plurality of memory banks, the subsets corresponding to different groups of audio channels.

4. (original)The method of claim 3 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

5. (canceled)

6. (previously presented) A system having first and second buses for processing real-time audio data from a plurality of audio channels, the system comprising:

a first processor and a second processor coupled to said first and second busses, respectively;

a plurality of memory banks of semiconductor memory devices coupled to said first and second buses for storing said audio data, said plurality of memory banks being accessible to the first and second processors for operations selected from the group comprising read and write operations, said plurality of memory banks storing subsets of audio data, said subsets corresponding to different groups of audio channels; and

a plurality of selectors coupled said first and second buses to select said memory banks for access by one of said first and second processors.

7. (previously presented) The system of claim 6 wherein the plurality of selectors include a plurality of address multiplexers and data transceivers.

8. (previously presented) The system of claim 6 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

9. (previously presented) The system of claim 6, wherein the memory banks include dynamic random access memories.

10. (previously presented) The method of claim 3, wherein storing further comprises interleaving the subsets of data.

11. (previously presented) The system of claim 6, wherein the subsets are stored in the memory banks in an interleaving manner.

12. (previously presented) The method of claim 3, wherein storing comprises storing one of the subsets of audio data in one of the memory banks, said method further comprising reading stored audio data from a second of the memory banks.

13. (previously presented) The method of claim 3, wherein the first processor performs a read operation on a first memory bank of the plurality of memory banks and the second processor performs a write operation on a second memory bank of the plurality of memory banks.

14. (previously presented) The system of claim 6, wherein subsets of audio data are stored in one of the memory banks and stored audio data is read from a second memory bank of the memory banks.

15. (previously presented) The system of claim 6, wherein the first processor performs a read operation on a first memory bank of the plurality of memory banks and the second processor performs a write operation on a second memory bank of the plurality of memory banks.

AF/2644

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	08/936,344
Filing Date	September 24, 1997
First Named Inventor	Paul Michael Embree
Art Unit	2644
Examiner Name	Minsun Harvey
Total Number of Pages in This Submission: 17	Attorney Docket Number: 80398P115

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below):*

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Thinh V. Nguyen, Reg. No. 42,034 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	January 9, 2004

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	**Tu T. Nguyen**		
Signature		Date	**January 9, 2004**

Based on PTO/SB/21 (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 09/11/2003.
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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	08/936,344
Filing Date	September 24, 1997
First Named Inventor	Paul Michael Embree
Examiner Name	Minsun Harvey
Group/Art Unit	2644
Attorney Docket No.	80398P115

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

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☒ Charge any additional fee(s) required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims		- 20** =		X		=	
Independent Claims		- 3 =		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple Dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater, For Reissues, see below*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	1,210	2255	605	Extension for reply within fifth month	
1404	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	1809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Thinh V. Nguyen	Registration No. (Attorney/Agent)	42,034	Telephone	(714) 557-3800
Signature				Date	01/09/04

Based on PTO/SB/17 (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 08/11/2003.
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